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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

RAO, SHRINIVAS H

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/574,829	Applicant(s) YAMAZAKI ET AL.	
	Examiner STEVEN H. RAO	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 January 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Applicants' amendment filed on January 07, 2009 has been entered and forwarded to the examiner on January 7, 2009.

Therefore Claims 1 to 4, 7 and 13-14 as amended by the amendment and claims 5-6 and 8 to 12 as previously recited are currently pending in the Application.

Information Disclosure Statement

No further IDS after the one filed on April 06, 2006 (previously considered) has been filed in this case.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 to 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yudasaka et al. (U.S. Patent Publication No. 202/0179906, herein after Yudasaka, also cited by Applicants' in their IDS) in view of Bojkov et al. (U.S. Patent No. 5,947,783 herein after Bojkov)

With respect to claim1 Yudasaka describes a liquid crystal display device comprising: a pair of substrates (Yudasaka para 0003) ; a liquid crystal interposed between the pair of substrates; (Yudasaka para 0003)a thin film transistor over one of the pair of substrates; (Yudasaka para 0003 and a pixel electrode connected to the thin film transistor, wherein the thin film transistor comprises (fig. 17):

Yudasaka mentions a gate electrode but does not specifically mention it (gate) of nanoparticles.

However Bojkov a patent from the same filed of endeavor, describes in its abstract (co1.5 lines 30-35) a gate electrode formed over one of the substrates by fusing conductive nanoparticles to provide films that have desired pixel structures, that can be

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used in display structures.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Bojkov's a gate electrode formed over the substrate by fusing conductive nanoparticles in Yudasak's device. The motivation for the above inclusion is to provide films that have desired pixel structures, that can be used in display structures. (Bojkov col.1 lines 43-47).

The remaining limitations of Claim 1 are :

A first layer including at least one of silicon nitride and silicon oxynitride formed on and in direct contact with the gate electrode, (Bojkov fig. 6,22) a gate insulating layer at least containing a second layer comprising silicon oxide over the first layer, (Bojkov col. 3 lines 14-15) and a semiconductor layer over the gate insulating layer. (Bojkov fig.6 # 600).

With respect to claim 2 Yudasaka describes a liquid crystal display device comprising: a pair of substrates, a liquid crystal interposed between the pair of substrates; a thin film transistor over one of the pair of substrates; and a pixel electrode connected to the thin film transistor, wherein the thin film transistor comprises: a gate electrode formed over one of the substrate by fusing conductive nanoparticles, a first layer including at least one of silicon nitride and silicon oxynitride formed on and in direct contact with the gate electrode, a gate insulating layer at least containing a silicon oxide layer over the first layer, and a semiconductor layer over the gate insulating layer; (rejected for reasons under claim1 above) a wiring connected to at least one of a source and a drain; (Yudasaka para 0188, fig~4) and a second layer including at least one of silicon nitride and nitride oxide formed to be on and in direct contact with the wiring (Bojkov col.3 lines 14--15), wherein the wiring formed by fusing conductive nanoparticles. (Bojkov col. 5 lines 30-35).

With respect to claim 3 Yudasaka describes a liquid crystal display device comprising: a pair of substrates; a liquid crystal interposed between the pair of substrates; a first thin film transistor over one of the pair of substrates; a pixel electrode connected to the thin film transistor; a driver circuit constructed by a second thin film transistor which comprises the same layer structure of the first thin film transistor; and a wiring extending from the driver circuit and connected to a gate electrode of the first thin film transistor, wherein the first thin film transistor comprises: the gate electrode formed over one of the substrates by fusing conductive nanoparticles, (rejected for reasons under claim1 above) a first layer including at least one of silicon nitride and nitride oxide silicon formed on and in direct contact with the gate electrode, a gate insulating layer at least containing a layer comprising silicon oxide over the layer, and a semiconductor layer over the gate insulating layer. (rejected for reasons under claims1 -2 above).

With respect to claim 4 Yudasaka describes a liquid crystal display device comprising: a pair of substrates; a liquid crystal interposed between the pair of substrates; a first thin

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film transistor over one of the pair of substrates; a pixel electrode connected to the thin film transistor; a driver circuit constructed by a second thin film transistor which comprises the same layer structure of the first thin film transistor and a first wiring extending from the driver circuit and connected to a gate electrode of the first thin film transistor, wherein the first thin film transistor comprises :

The gate electrode formed over one of the substrates by fusing conductive nano particles , a first layer including at least one of silicon nitride and nitride oxide silicon formed on and in direct contact with the gate electrode, a gate insulating layer at least containing a silicon oxide layer over the first layer, and a semiconductor layer over the gate insulating layer; a second wiring connected to at least one of a source and a drain; formed on and in direct contact with the second wiring, wherein the second wiring formed by fusing conductive nanoparticles. (rejected for reasons under claim 1-3 above).

With respect to claim 5 Yudasaka describes the liquid crystal display device according to any one of claims 1 to 4, wherein the conductive nanoparticles comprise Ag. (well known in the art).

With respect to claim 6 Yudasaka describes the liquid crystal display device according to claim 2 or 4, wherein the semiconductor layer comprises at least one of hydrogen and halogen; and wherein the semiconductor layer is a semi- amorphous semiconductor having a crystal structure. (Yudasaka para 00135).

With respect to claim 7 Yudasaka describes the liquid crystal display device according to claim 3 or 4, wherein the driver circuit comprises only an n-channel type thin film transistor.

With respect to claim 8 Yudasaka describes the liquid crystal display device according to claim 1 or 2, wherein the thin film transistor comprises the semiconductor layer including hydrogen and halogen and which is a semiconductor having a crystal structure, wherein the thin film transistor is capable of being operated in electric field effect mobility of from 1 cm²N-sec to 15 cm²N-sec.

With respect to claim 9 Yudasaka describes liquid crystal display device according to claim 3 or 4, wherein the first thin film transistor and the second thin film transistor comprise the semiconductor layer including hydrogen and halogen and which is a semiconductor having a crystal structure, wherein the first thin film transistor and the second thin film transistor are capable of being operated in electric field effect mobility of from 1 cm²N-sec to 15 5 cm²N-sec. (Bojkov col.3 lines 64-67, Yudasaka para 00197).

With respect to claim 10 Yudasaka describes a liquid crystal television receiver comprising the liquid crystal display device according to any one of claims 1 to 4.

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(rejected for reasons under claims 1 to 4).

With respect to claim 11 Yudasaka describes a method for manufacturing a liquid crystal display device comprising the steps of: forming a gate electrode over a substrate having an insulating surface with a droplet discharge method; laminating a gate insulating layer, a semiconductor layer, and an insulating layer over the gate electrode; (rejected for reasons under claims 1 to 4 above) forming a first mask in a position overlapping with the gate electrode with a droplet discharge method; forming a channel protective layer by etching the insulating layer by using the first mask; (Yudasaka para 0183) forming a semiconductor layer containing one conductivity type impurity; (Yudasaka figs.) forming a second mask in a region including the gate electrode with a droplet discharge method; etching the semiconductor layer containing one conductivity type impurity and the semiconductor layer; (Yudasaka para 00186) forming source and drain wirings with a droplet discharge method; (Yudasaka fig. 11 33s and 33d) and etching the semiconductor layer containing one conductivity type impurity over the channel protective layer by using the source and drain wirings as masks. (Yudasaka para 0187)

With respect to claim 12 Yudasaka describes a method for manufacturing a liquid crystal display device comprising the 30 steps of: forming a gate electrode and a connection wiring over a substrate having an insulating surface with a droplet discharge method; laminating a gate insulating layer, a semiconductor layer, and an insulating layer over the gate electrode; forming a first mask in a position overlapping with the gate electrode with a droplet discharge method; forming a channel protective layer by etching the insulating layer by using the first mask; forming a semiconductor layer containing one conductivity type impurity; forming a second mask in a region including the gate electrode with a droplet discharge method; etching the semiconductor layer containing one conductivity type impurity and the semiconductor layer; partially exposing the connection wiring by selectively etching the gate insulating layer; forming a source wiring and a drain wiring and connecting at least one of the source wiring and the drain wiring to the connection wiring at the same time; and etching the semiconductor layer containing one conductivity type impurity over the channel protective layer by using the source and drain wirings as masks. (rejected for reasons under claims 1-4 and 12).

With respect to claim 13 Yudasaka describes the method for manufacturing a liquid crystal display device according to claim 11 or 12, wherein the step of laminating a gate insulating layer, a semiconductor layer, and an insulating layer over the gate electrode is carried out without exposing to the atmosphere. (para 0039 e.g. CVD carried out in enclosed chamber).

With respect to claim 14 Yudasaka describes the method for manufacturing a liquid crystal display device according to claim 11 or 12, wherein the gate insulating film is sequentially laminated by a first silicon nitride film, a silicon oxide film, and a second silicon nitride film. (Bojkov co13 lines 14--15).

Response to Arguments

1. Applicant's arguments filed April 06, 2006 have been fully considered but they are not persuasive for the following reasons :

2. Applicants' first contention that either the applied Yudasaka or Bojkov references do not either alone or in combination do not allegedly teach various cited portions of claims 1-4, 11 and 12 on pages 7-8 of their response of Jan. 07, 2009 is not persuasive for reasons set out in the rejection above and incorporated here by reference for sake of brevity.

3. Applicants' specific contention that the Applied Bojkov reference does not describe a gate electrode formed over a substrate by fusing conductive nano particles is not persuasive because as admitted to by the Applicants and at least Attorney Mark w. Butler (50,219) in their response Bojkov in col. 5 lines 41-50 describes diamond particles (nano-size) being deposited on metal strip and form future center of diamond growth , which diamond coating on the metal layer forms cathode layer 201 (an electrode) e.g. figure 6 (reproduced below).

4.

The process of selectively seeding diamond particles onto the cathode strips 1102 is illustrated in FIG. 16. The cathode comprising substrate 1101 and metal strips 1102 is placed in a container 1601 containing an organic alcohol solution (isopropyl alcohol, methanol, etc.) 1602, which also contains a charging salt such as $\text{Al}(\text{NO}_3)_3$ or $\text{Mg}(\text{NO}_3)_2$ or $\text{La}(\text{NO}_3)_3$. The anode 1603 may be nickel, stainless steel, or platinum. Diamond particles of a nano-size (powder) are dispersed into solution 1602. Upon applying a negative voltage using power supply 1605 and monitored by voltmeter 1604, onto the cathode, the diamond particles are electrophoretically deposited onto metal lines 1102, thus forming the future centers for preferential diamond growth.

The result of this process is illustrated in FIG. 17, which illustrates such nano-size diamond particles 1701 deposited onto metal lines 1102.

Next, the cathode structure illustrated in FIG. 17 is introduced into a vacuum chamber for chemical vapor deposition (CVD) of diamond, using a process well-known in the art. The process of diamond nucleation occurs primarily onto the diamond particles 1701 forming continuous diamond layer 1801 (FIG. 18). The result of this process is that the areas denoted by the dashed circles 1802 have a much higher resistance than the diamond layer portions residing above the metal lines 1102. This effectively reduces, or eliminates cross-talk between metal lines 1102.

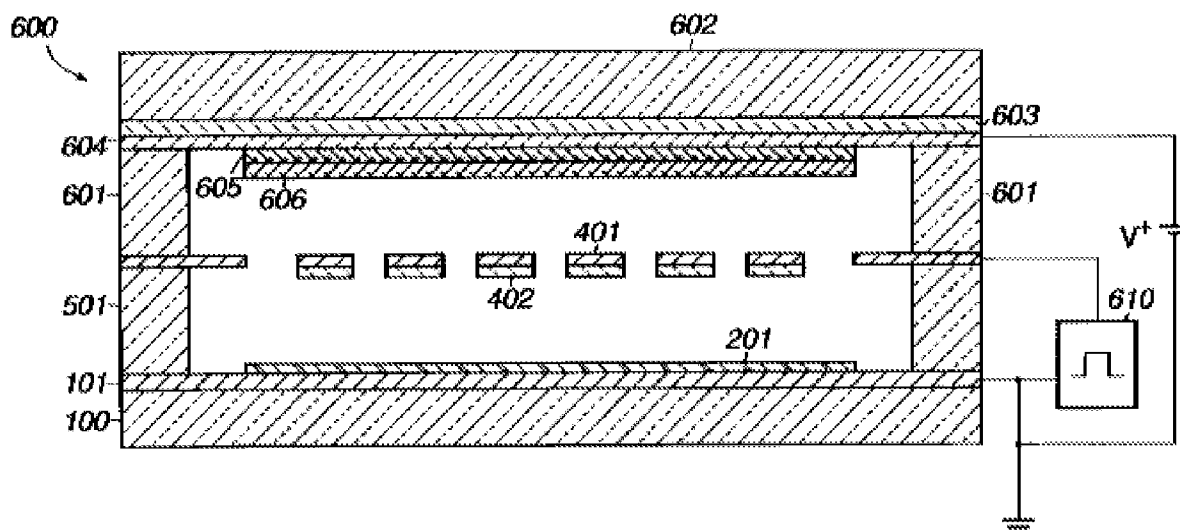


Fig. 6

Therefore Applicants' and their attorney's conclusion that Bojkov does not describe a gate electrode formed over a substrate by fusing conductive nano particles is simply wrong and not supported by facts.

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Applicants' second contention that, " Borkov describes that the result of the process effectively reduces or eliminates cross-talk between metal lines 102, it should be regarded that diamond is not conductive and in fact teaches away from the claimed invention" is not persuasive because it seems and attorney butler did not understand the teachings of Borkov.

Applicants' and attorney freely admit that Borkov describes that diamond particles are electrophoretically deposited on to metal lines 1102 (cathode stripe" (Applicants' response page 9 lines 1-3).

As one skilled in the art would understand that Electrophoretic deposition is a process wherein :

"The migration of charged colloidal particles or molecules through a solution under the influence of an applied electric field usually provided by immersed electrodes also called cataphoresis " (emphasis supplied).

Therefore Applicants' etc. should understand the diamond particles (nano size) of Borkov would not deposited on metal strip (electrode) unless they are charges particles or molecules (i.e. conducting) by electrophoresis as admitted by the above stated. .

Therefore Applicants' contention "that Borkov's description , it should be regarded that diamond is not conductive and in fact teaches away from the claimed invention " is not supported by facts.

On the contrary as charged particles molecules they are conducting and in fact teach the combination.

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Therefore Bojkov reference teaches as applied teaches and fairly discloses to one of ordinary skill in the art that the gate electrode is formed over the substrate by fusing conductive nano particles as recited in claims 1 to 4.

Applicants' contention with regard to claims 11 and 12 that Yudasaka does not allegedly disclose or fairly teach forming a gate electrode over the substrate having an insulating surface with a droplet discharge method, is also not persuasive.

As stated above under claim 1-4 above for reasons set out in detail therein Bojkov reference teaches as applied teaches and fairly discloses to one of ordinary skill in the art that the gate electrode is formed over the substrate. Further Yudasaka in col. 20 lines 25-30 (reproduced below):

... is effectively used. This process is also applicable to the formation of the insulating film, silicon film and conductive film instead of the coating process, and thus greatly contributes to cost reductions of liquid crystal display devices.

Therefore a correct reading of Yudasaka shows that not only forming a resist but also a silicon film and a conductive film both of which can be used a gate electrode, further one of ordinary skill in the art would understand from Yudasaka's figs. e.g. 3-16 and reading col. 20 lines 23-25 (reproduced below)

... The resist coating process is an ink jet-type liquid coating process and the resist is applied onto the entire substrate as dots. Because the substrate is moved or rotated so as to apply

That the resist, silicon or conductive material is applied as dots i.e. droplet discharge method is used.

Therefore the combination of Yudasaka and Bojkov describes all the presently recited elements/steps of claims 1 and 12.

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It is not understood how applicants' and Attorney Butler can conclude that the Examiner failed to establish prime facie case of obviousness for at least four reasons.

As shown in the rejection above the Examiner has demonstrated to one of ordinary skill in the art how Yudasaka and Bojkov alone or in combination disclose or suggest each and every feature presently recited in the claims .

Secondly, the Examiner has shown probability of success by at least combining two patents from the same field of endeavor.

Thirdly, the Examiner has identified and stated in writing the motivation to modify Yudasaka with teachings of Bojkov (reproduced below) in the teachings of the applied references itself (e.g. Bojkov col.1 lines 43-47).

“Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Bojkov's a gate electrode formed over the substrate by fusing conductive nanoparticles in Yudasaka's device. The motivation for the above inclusion is to provide films that have desired pixel structures, that can be used in display structures. (Bojkov col.1 lines 43-47). “

Therefore the Applicants and attorney did not fully read the previous rejection or merely cut and paste boiler plate arguments whether they are applicable to this case or not.

Finally the above clearly shows the how the Examiner's rationale for obviousness is found in prior art and is not a hindsight reconstruction of Applicants' own disclosure.

Applicants' and their attorneys are reminded that the standard for rejections is that it should be understood by one of ordinary skill in the art and the Office and the Examiner cannot be expected and is not required by current law to provide rejections that is understood by every applicant and their attorneys.

Therefore Yudasaka and Bojkov disclose all the presently recited elements. Dependent Claims were alleged to be allowable because of their dependency upon allegedly allowable independent claims. However as shown above independent Claims are not allowable, therefore dependent claims are also not allowable.

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5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN H. RAO whose telephone number is (571)272-1718. The examiner can normally be reached on 8.30-5.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Howard Weiss/
Primary Examiner, Art Unit 2814

/Steven H Rao/
Examiner, Art Unit 2814